

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):

Takayuki NOTO et al.

Serial No.:

Not Yet Assigned

Filed:

July 20, 2005

For:

SEMICONDUCTOR INTEGRATED CIRCUIT

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 & 1.98

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 July 20, 2005

Sir:

In the matter of the above-identified application, applicant(s) are submitting herewith a copy of the documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted with the new application.

To the extent that the documents listed on the attached form equivalent to Form PTO-1449 are not in the English language, the requirement of 37 CFR 1.98(a)(3) for a concise explanation of the relevance is satisfied by an English abstract and/or the discussion of these documents in the specification.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (1374.45249X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

Gregory E. Montone Registration No. 28,141

ANTONELLI, TERRY, STOUT & KRAUS, LLP

GEM/dc Attachments (703) 312-6600

10/542727 1012 Rec'd PCT/PTC 20 1111 2005

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1374.45249X00

App or use through 07/31/2006. OMB 0651-0031
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INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

Application Number
Filing Date
July 20, 2005
First Named Inventor
Art Unit
Examiner Name

Attorney Docket Number

of

Sheet

			U.S. PATENT I		
Examiner Initials'	Cite No.1	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS						
Examiner Initials'	Cite No.1	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		JP 2-235435	9/18/1990	Nec Corp		Abs
		JP 5-14169	1/22/1993	Nec Corp		Abs
		JP 3-62723	3/18/1991	Nec Corp	-	Abs
		JP 3-232020	10/29/1991	Nec Corp		Abs

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
		Takayuki KAWAHARA et al., "Low-Power Chip Interconnection by Dynamic Termination", IEEE J. of Solid-State Circuits, Vol. 30, No. 9, 30 September 1995 (30.09.95), pages 1030 to 1034, Figs. 2, 3.	

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